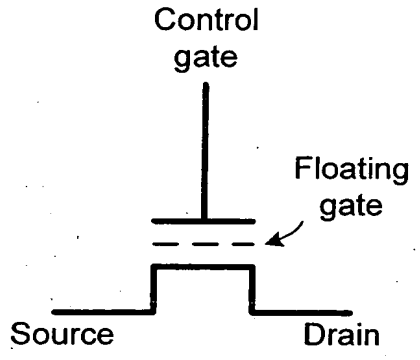

Control gate
Floating gate
Source
Drain

FIG. 1A

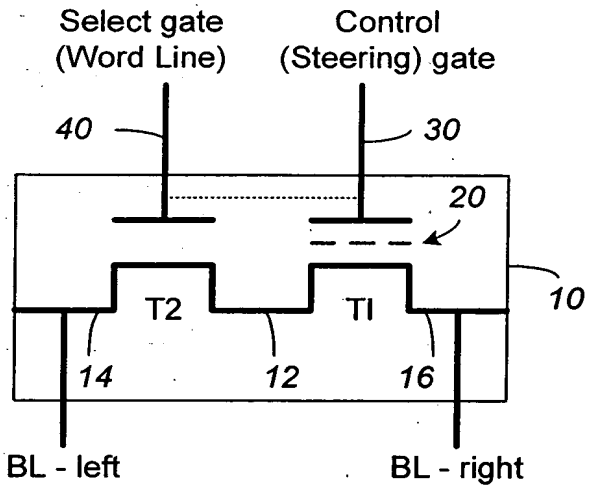

Select gate (Word Line)
Control (Steering) gate
40
30
20
10
T2
TI
14
12
16
BL - left
BL - right

FIG. 1B

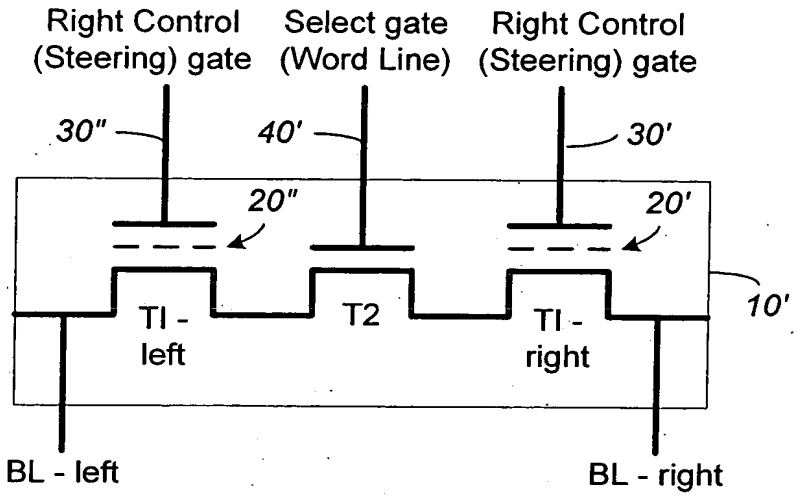

Right Control (Steering) gate
Select gate (Word Line)
Right Control (Steering) gate
30"
40'
30'
20"
20'
TI - left
T2
TI - right
10'
BL - left
BL - right

FIG. 1C

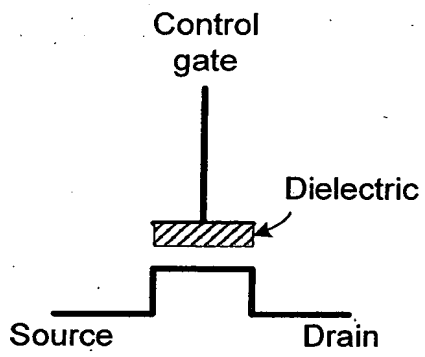

Control gate
Dielectric
Source
Drain

FIG. 1E

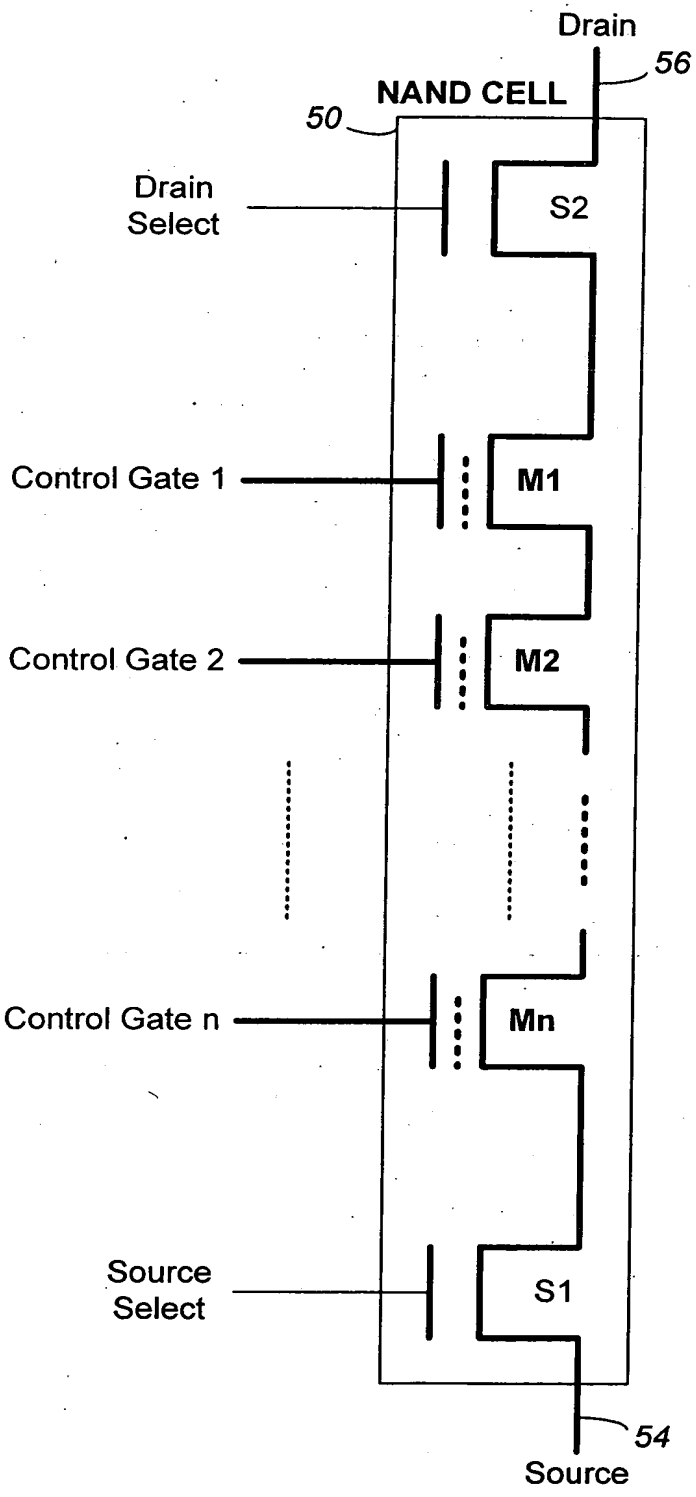

Drain
56
NAND CELL
50
Drain
Select
S2
Control Gate 1
M1
Control Gate 2
M2
Control Gate n
Mn
Source
Select
S1
54
Source

FIG. 1D

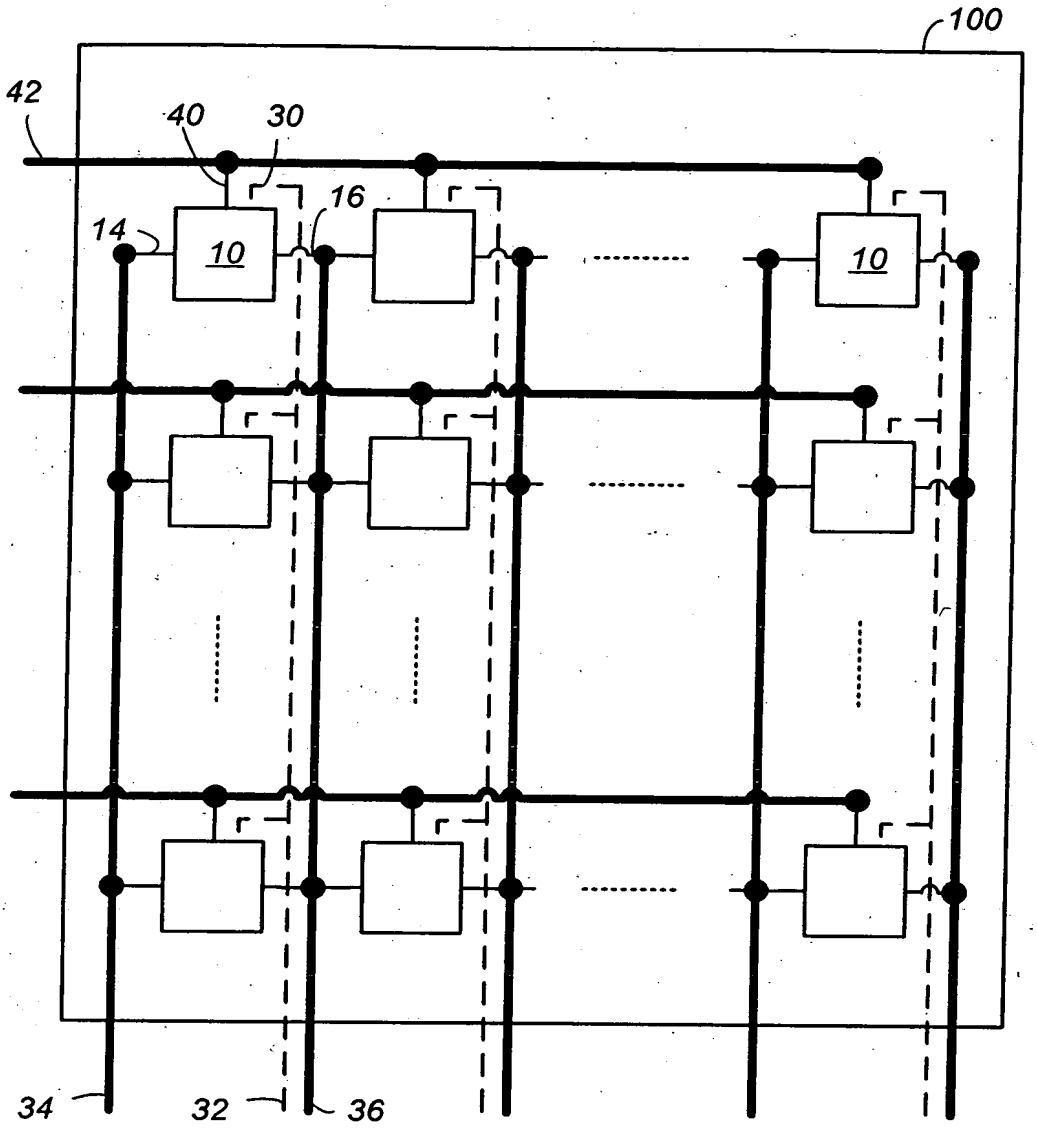


FIG. 2

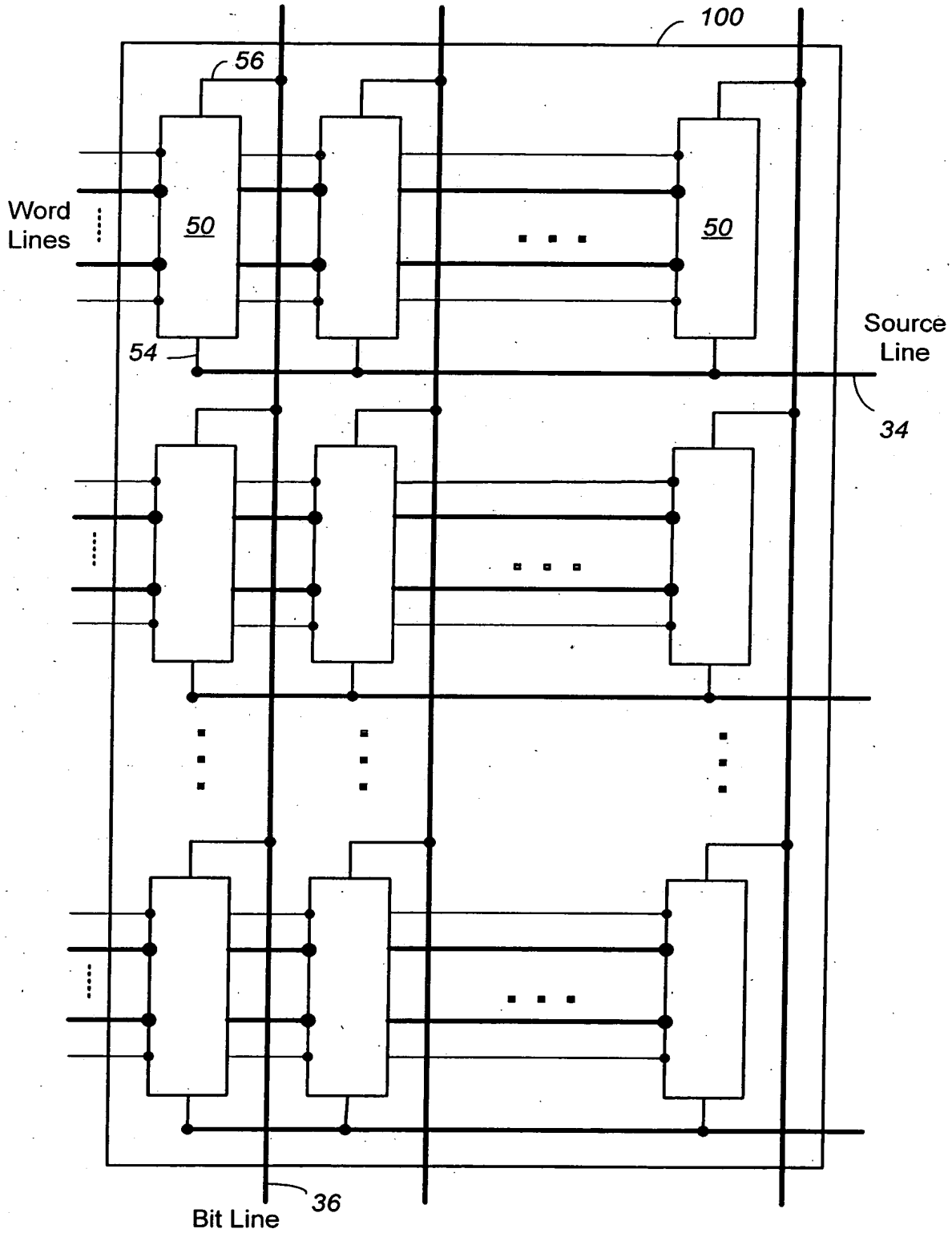


FIG. 3

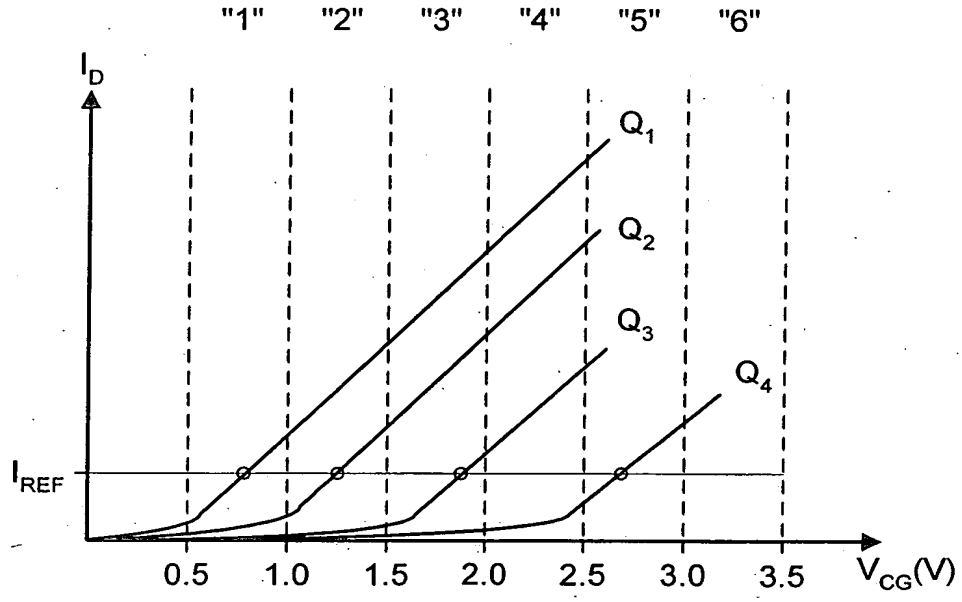


FIG. 4

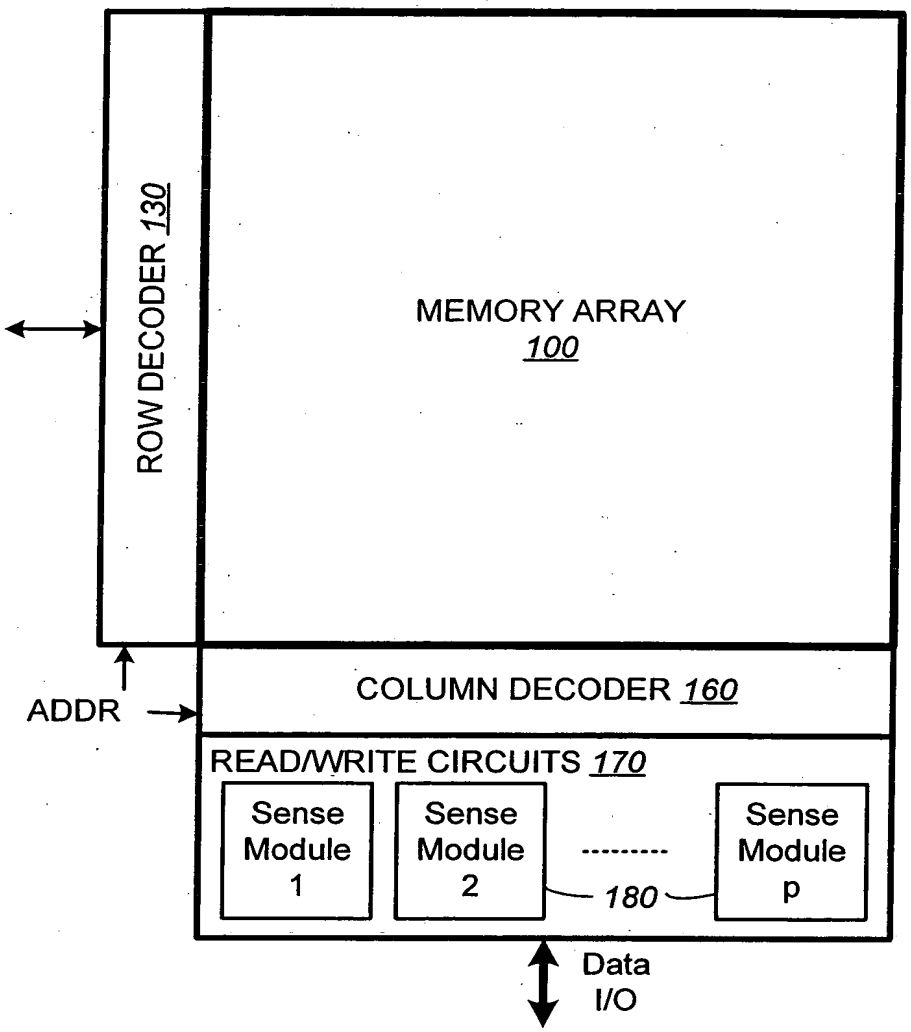

ROW DECODER 130
MEMORY ARRAY
100
ADDR
COLUMN DECODER 160
READ/WRITE CIRCUITS 170
Sense Module 1
Sense Module 2
Sense Module p
180
Data I/O

FIG. 5

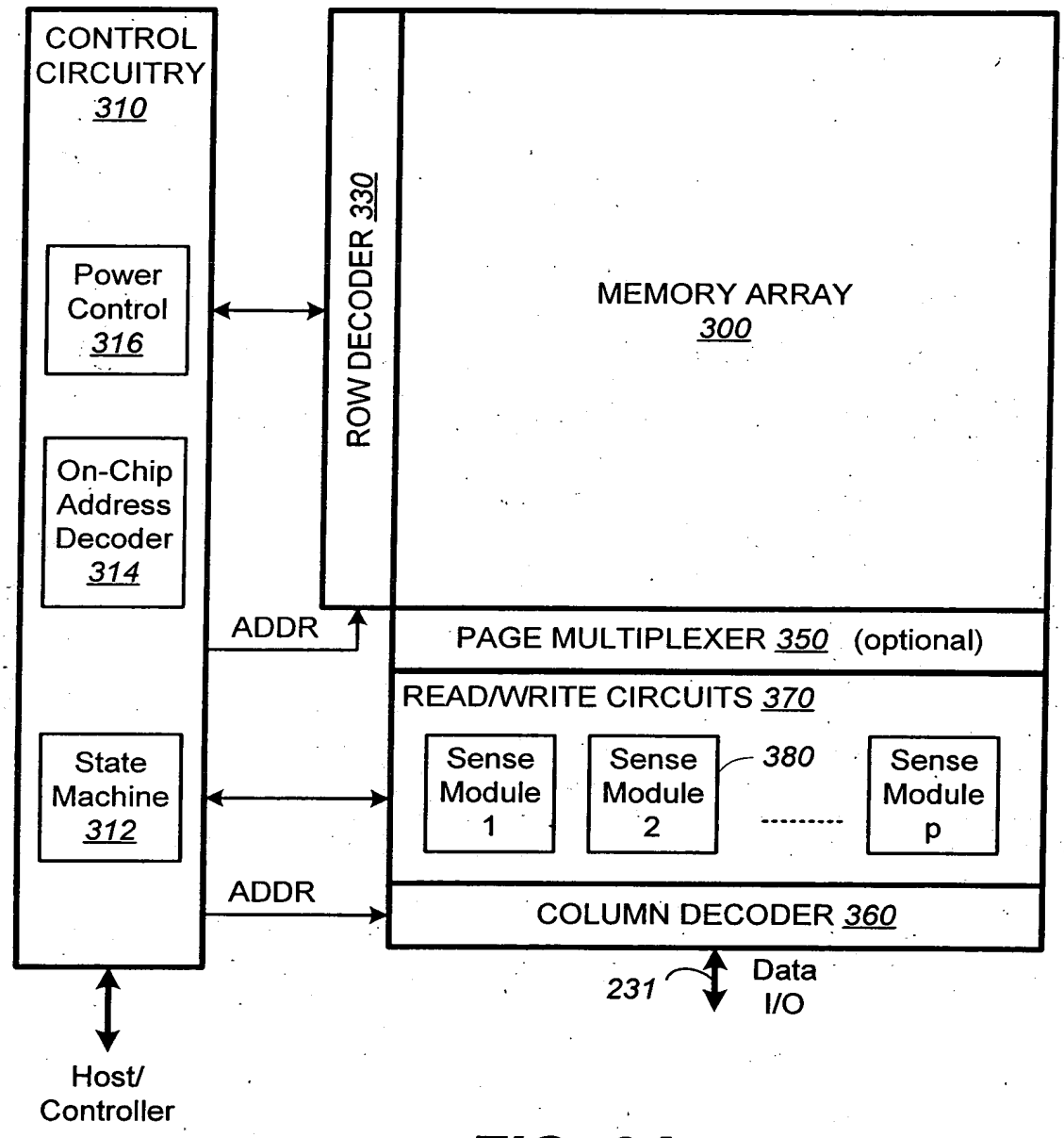

CONTROL CIRCUITRY 310
Power Control 316
On-Chip Address Decoder 314
State Machine 312
ROW DECODER 330
MEMORY ARRAY 300
ADDR
PAGE MULTIPLEXER 350 (optional)
READ/WRITE CIRCUITS 370
Sense Module 1
Sense Module 2
380
Sense Module p
ADDR
COLUMN DECODER 360
231
Data I/O
Host/ Controller

FIG. 6A

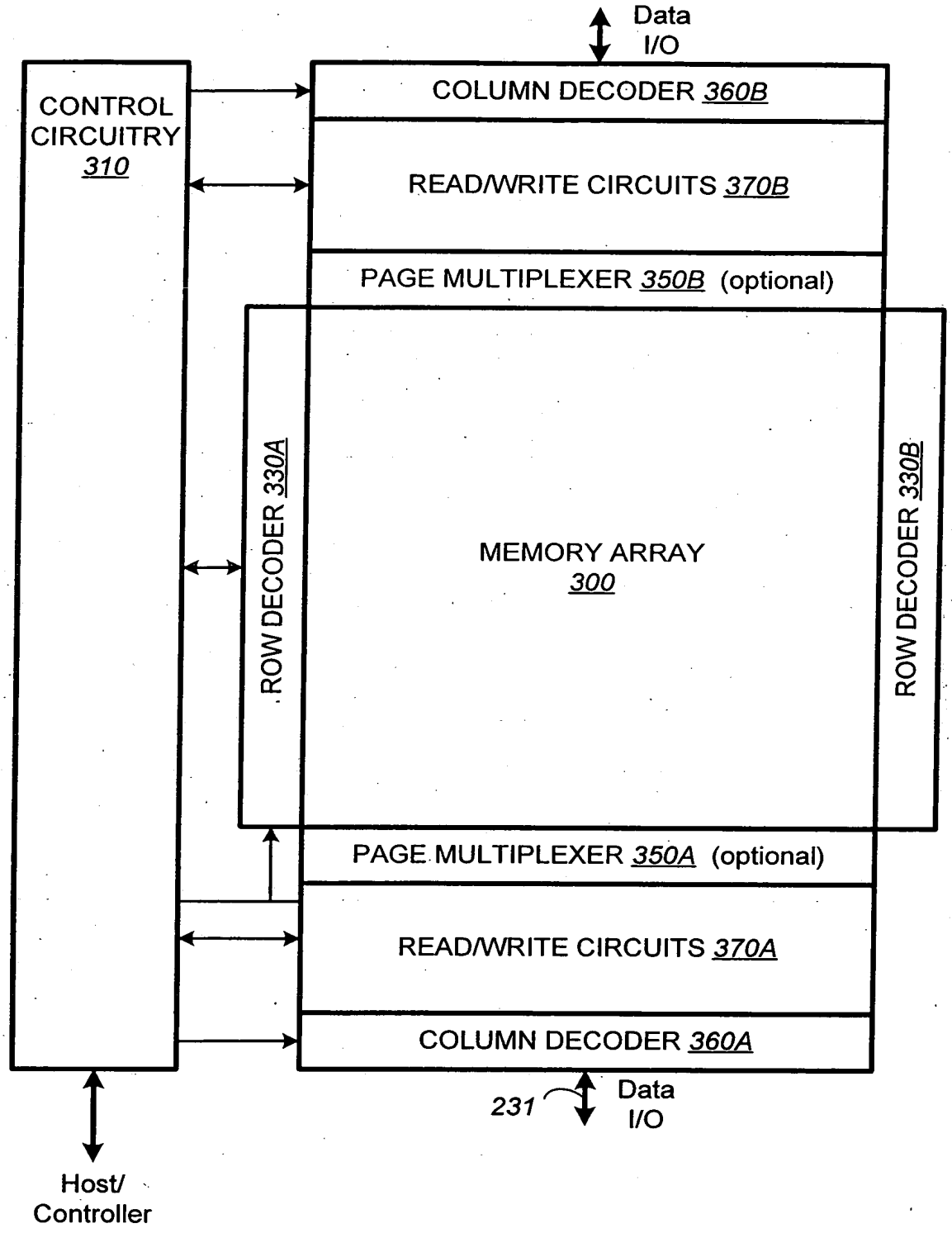

Data I/O
CONTROL CIRCUITRY 310
COLUMN DECODER 360B
READ/WRITE CIRCUITS 370B
PAGE MULTIPLEXER 350B (optional)
ROW DECODER 330A
MEMORY ARRAY 300
ROW DECODER 330B
PAGE MULTIPLEXER 350A (optional)
READ/WRITE CIRCUITS 370A
COLUMN DECODER 360A
231
Data I/O
Host/ Controller

FIG. 6B

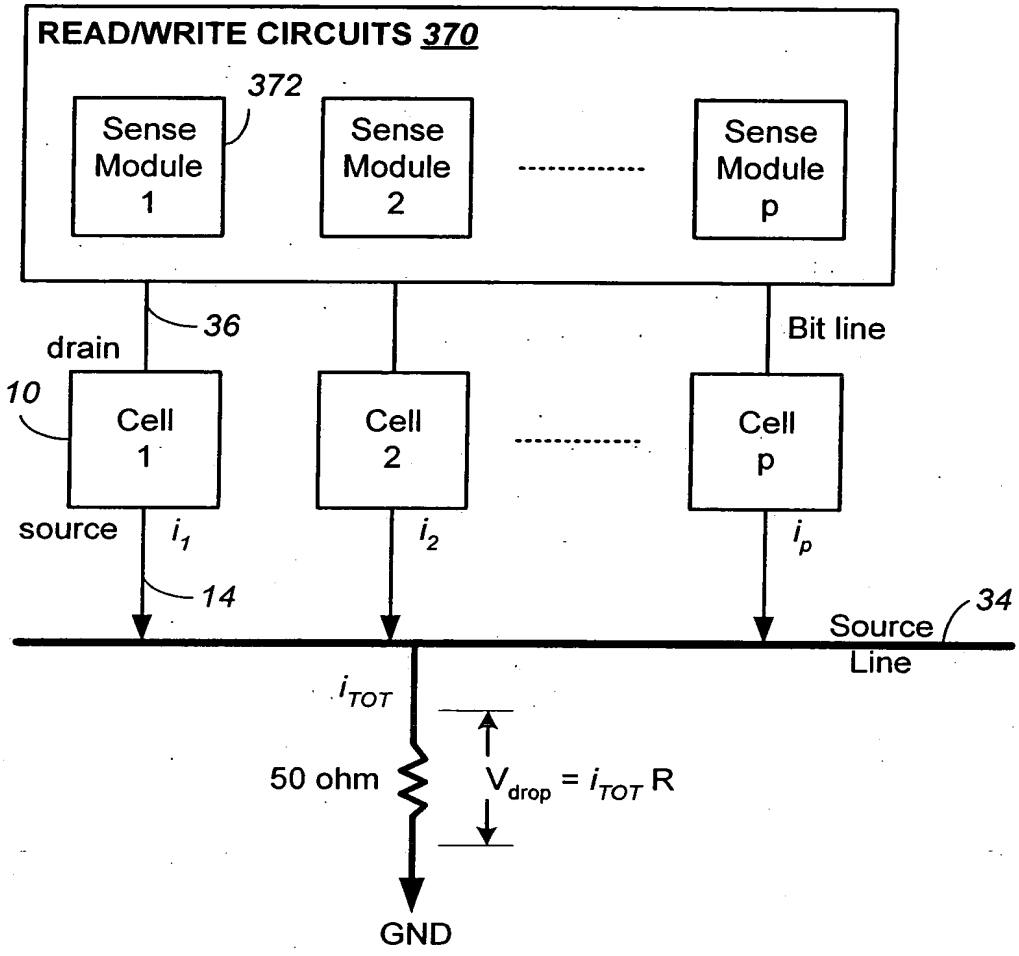

READ/WRITE CIRCUITS 370
372
Sense Module 1
Sense Module 2
Sense Module p
36
drain
Bit line
10
Cell 1
Cell 2
Cell p
source
i_1
i_2
i_p
14
34
Source Line
i_{TOT}
50 ohm
$V_{drop} = i_{TOT} R$
GND

FIG. 7A

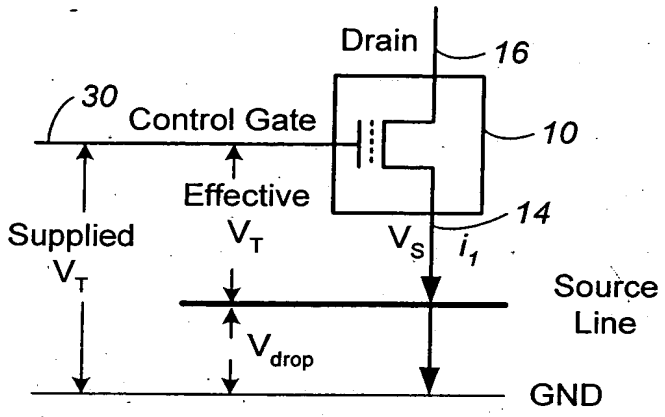

Drain
16
30
Control Gate
10
Effective
V_T
14
Supplied
V_T
V_S
i_1
Source
Line
V_{drop}
GND

FIG. 7B

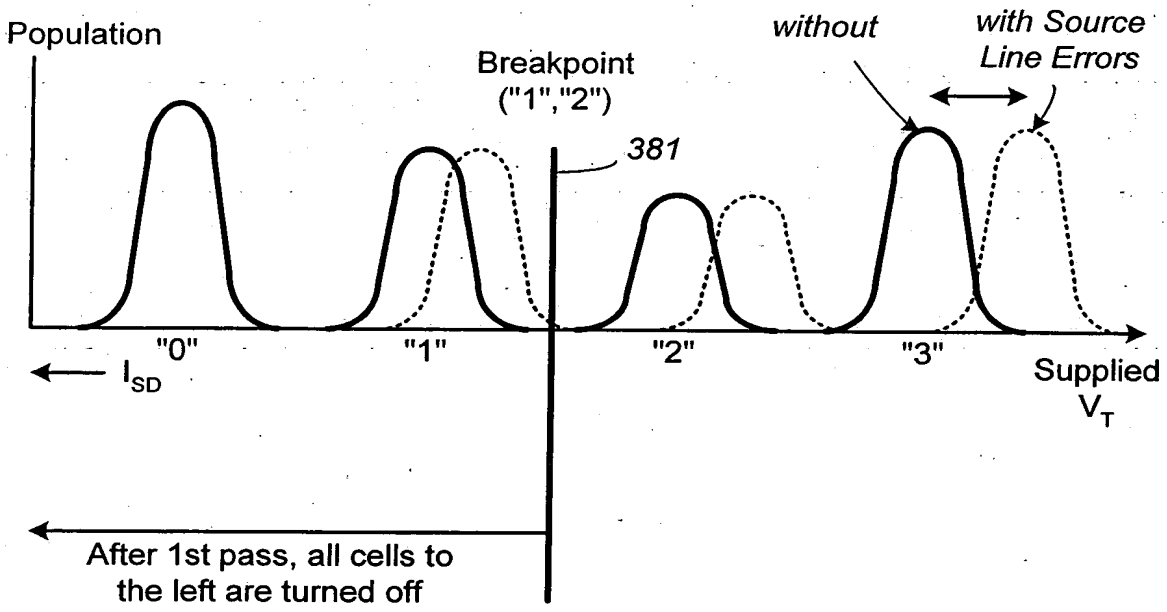

Population
Breakpoint
("1","2")
381
without
with Source
Line Errors
"0"
"1"
"2"
"3"
I_{SD}
Supplied
V_T
After 1st pass, all cells to
the left are turned off

FIG. 8

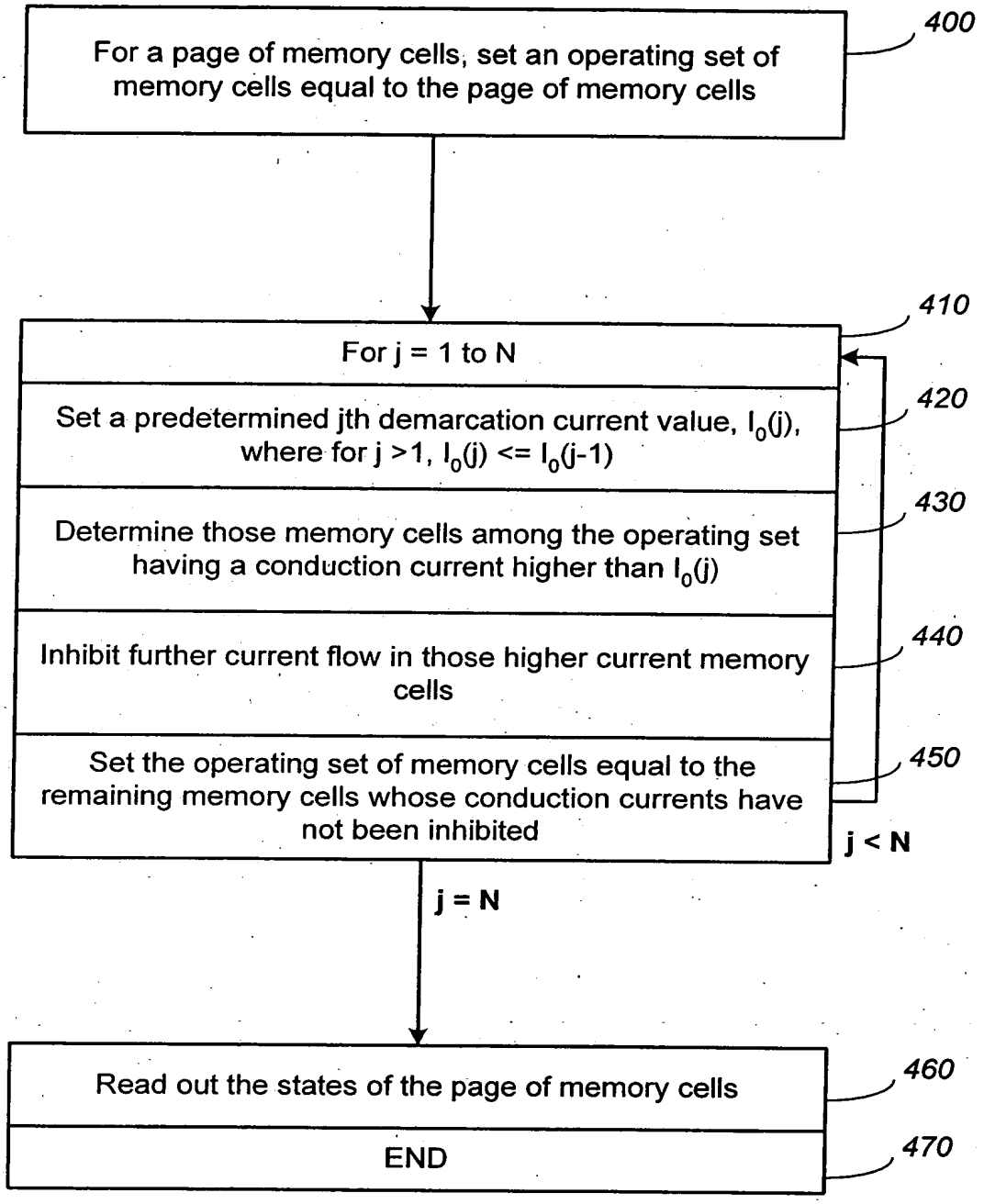

For a page of memory cells, set an operating set of memory cells equal to the page of memory cells
400
For j = 1 to N
410
Set a predetermined jth demarcation current value, $I_0(j)$, where for j >1, $I_0(j) <= I_0(j-1)$
420
Determine those memory cells among the operating set having a conduction current higher than $I_0(j)$
430
Inhibit further current flow in those higher current memory cells
440
Set the operating set of memory cells equal to the remaining memory cells whose conduction currents have not been inhibited
450
j < N
j = N
Read out the states of the page of memory cells
460
END
470

FIG. 9

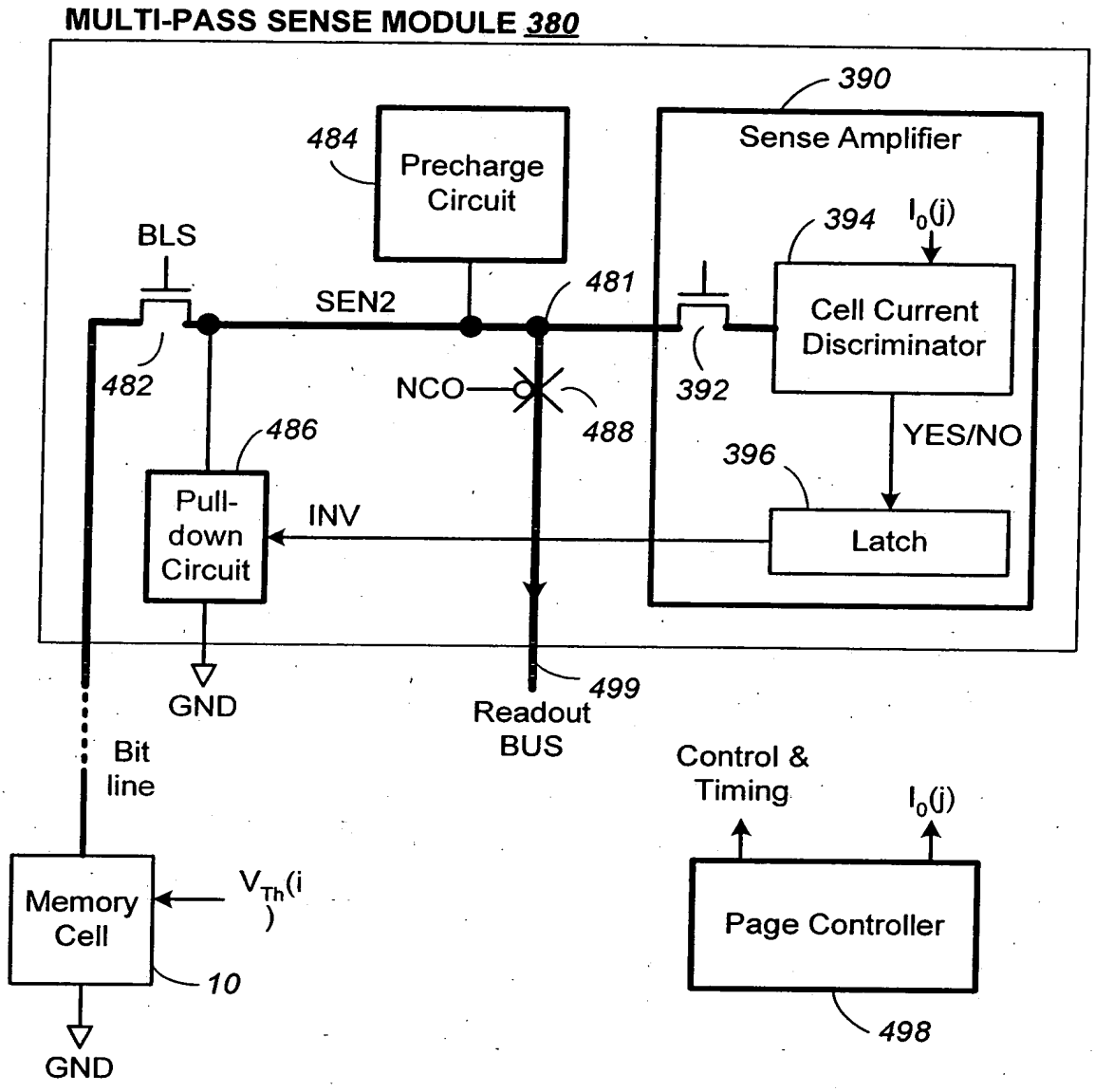

MULTI-PASS SENSE MODULE 380
390
Sense Amplifier
484
Precharge Circuit
394
$I_0(j)$
BLS
SEN2
481
Cell Current Discriminator
482
NCO
392
488
YES/NO
486
396
Pull-down Circuit
INV
Latch
GND
499
Readout BUS
Bit line
Control & Timing
$I_0(j)$
Memory Cell
$V_{Th}(i)$
10
Page Controller
498
GND

FIG. 10

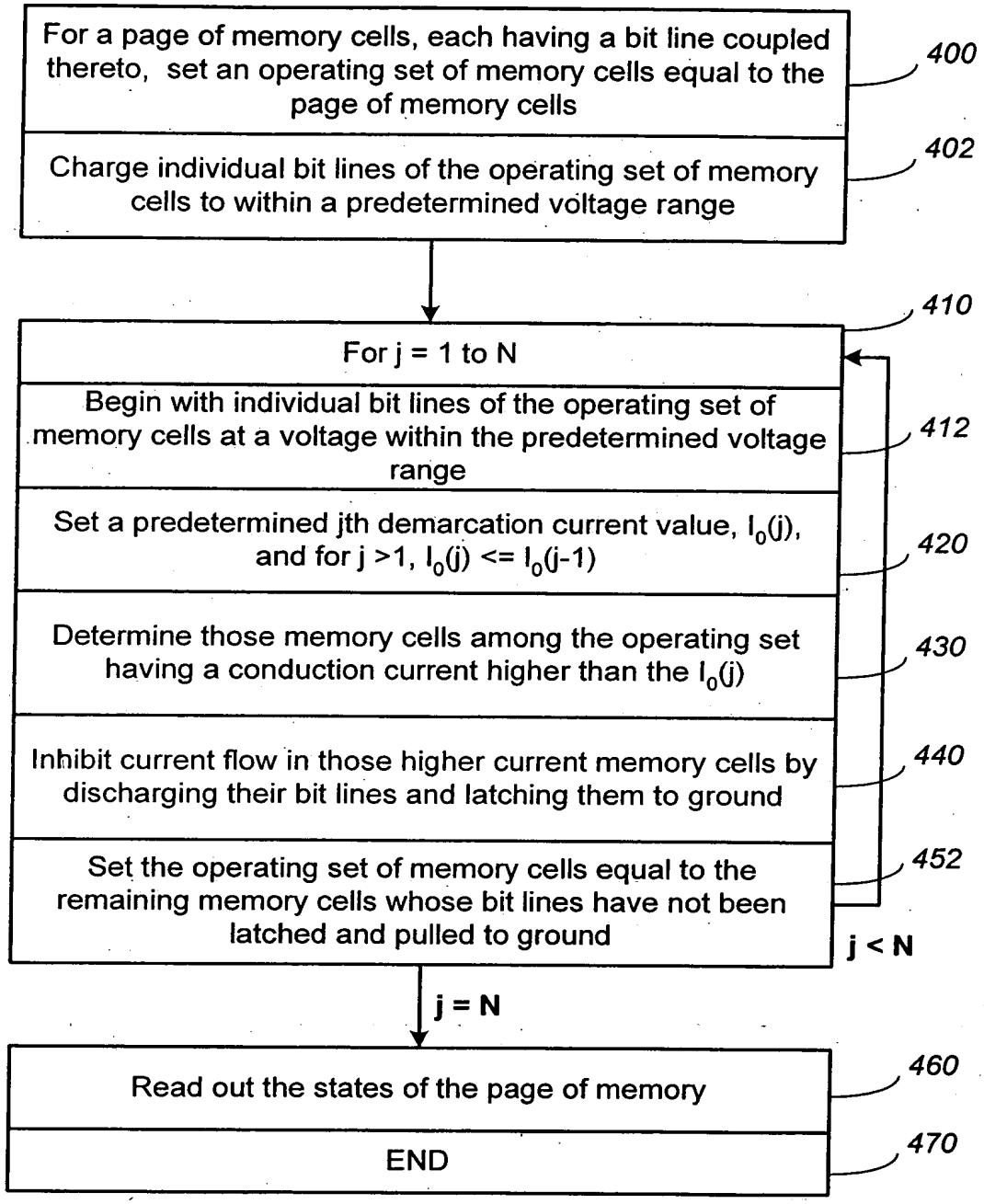
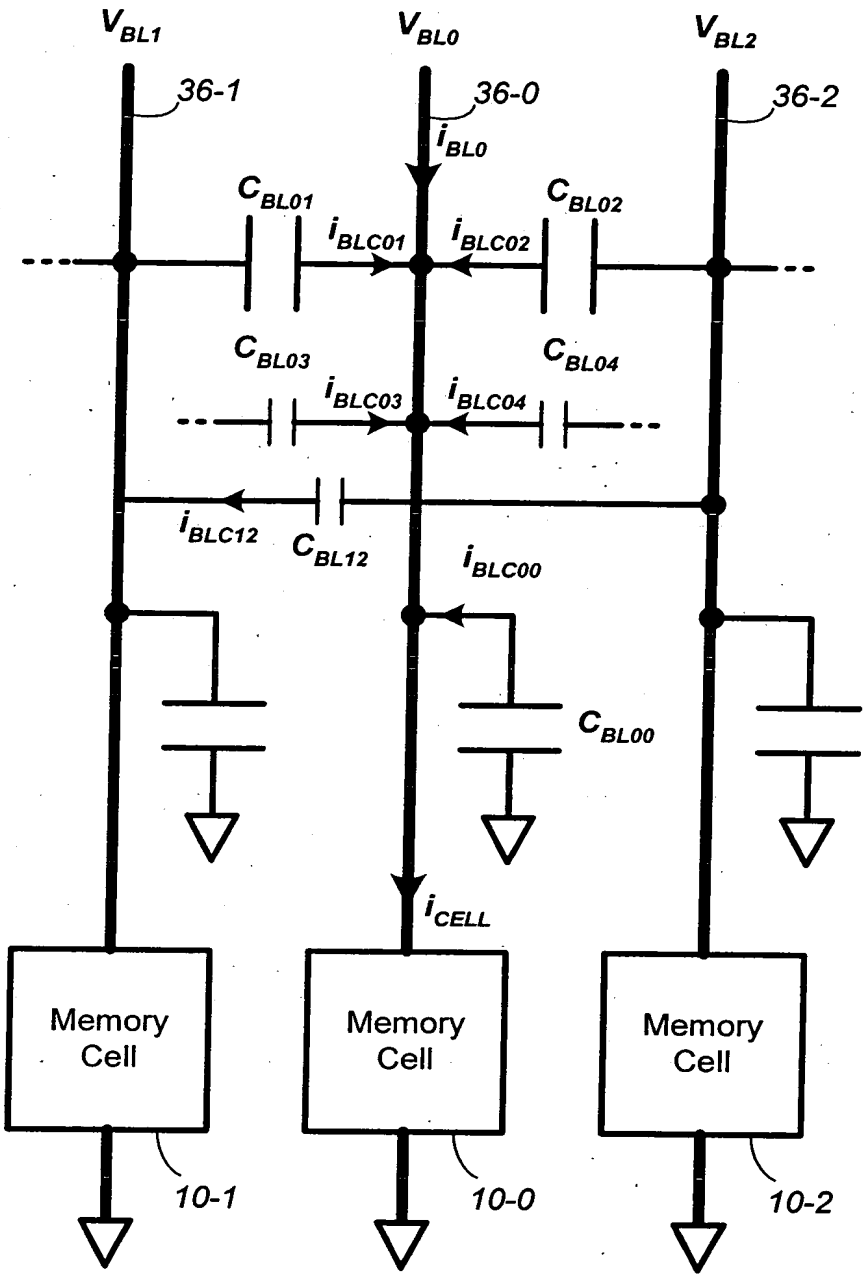

For a page of memory cells, each having a bit line coupled thereto, set an operating set of memory cells equal to the page of memory cells
400
Charge individual bit lines of the operating set of memory cells to within a predetermined voltage range
402
For j = 1 to N
410
Begin with individual bit lines of the operating set of memory cells at a voltage within the predetermined voltage range
412
Set a predetermined jth demarcation current value, $I_0(j)$, and for j >1, $I_0(j) <= I_0(j-1)$
420
Determine those memory cells among the operating set having a conduction current higher than the $I_0(j)$
430
Inhibit current flow in those higher current memory cells by discharging their bit lines and latching them to ground
440
Set the operating set of memory cells equal to the remaining memory cells whose bit lines have not been latched and pulled to ground
452
j < N
j = N
Read out the states of the page of memory
460
END
470

FIG. 11



$$i_{CELL} = i_{BL0} + [i_{BLC00} + i_{BLC01} + i_{BLC02} + i_{BLC03} + i_{BLC04}]$$

FIG. 12

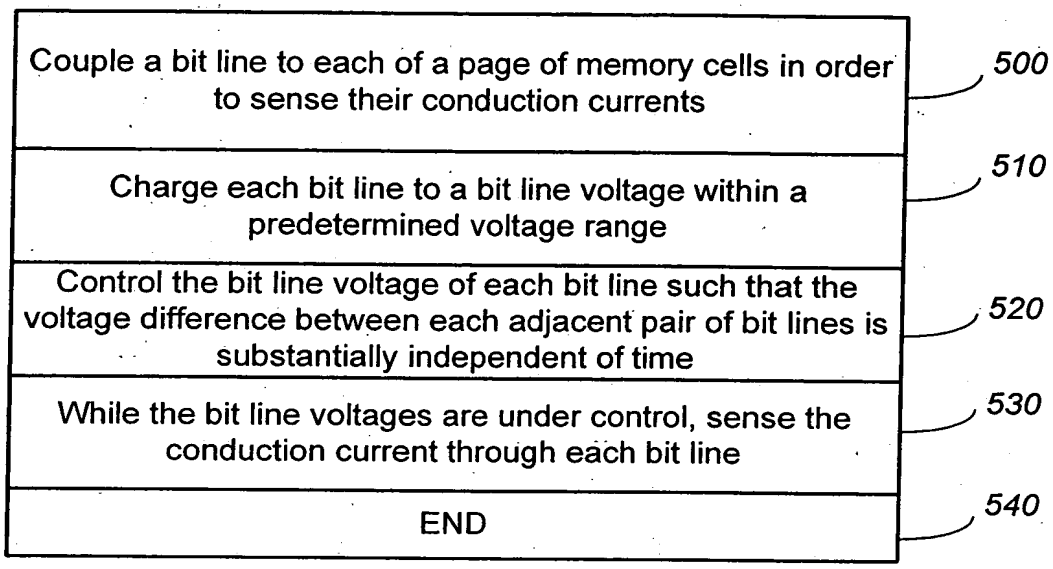

Couple a bit line to each of a page of memory cells in order to sense their conduction currents
500
Charge each bit line to a bit line voltage within a predetermined voltage range
510
Control the bit line voltage of each bit line such that the voltage difference between each adjacent pair of bit lines is substantially independent of time
520
While the bit line voltages are under control, sense the conduction current through each bit line
530
END
540

FIG. 13A

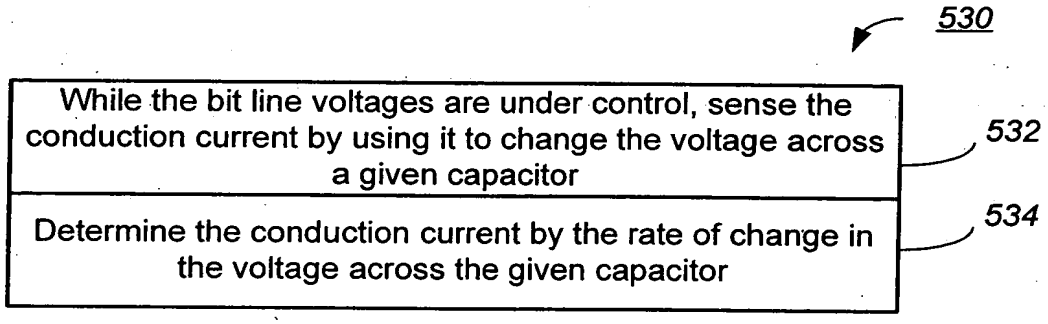

530
While the bit line voltages are under control, sense the conduction current by using it to change the voltage across a given capacitor
532
Determine the conduction current by the rate of change in the voltage across the given capacitor
534

FIG. 13B

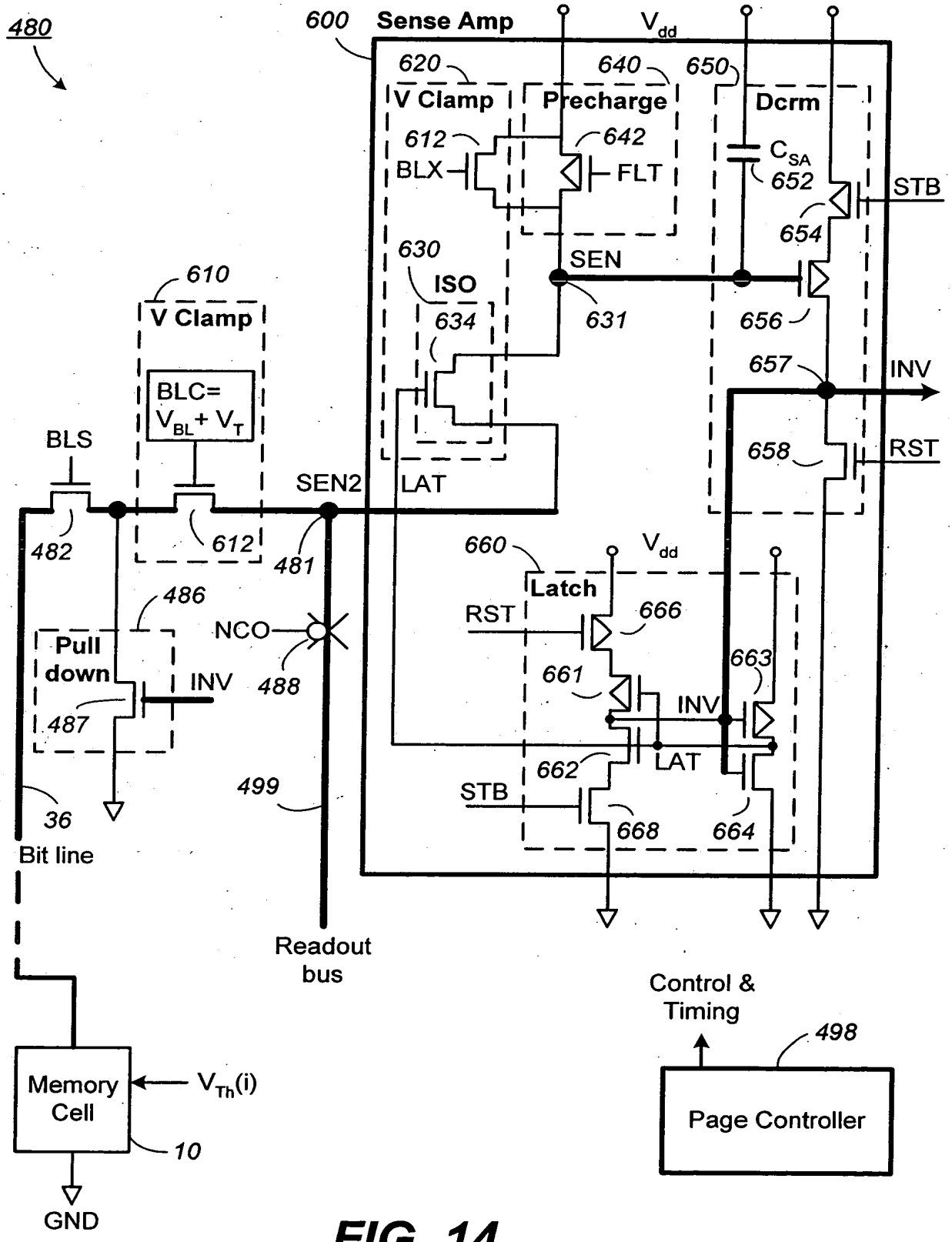

480
600
Sense Amp
V_{dd}
620
V Clamp
640
Precharge
650
Dcrm
612
BLX
642
FLT
C_{SA}
652
STB
654
630
ISO
SEN
631
656
610
V Clamp
634
657
INV
BLC=
$V_{BL}+V_T$
BLS
658
RST
SEN2
LAT
482
612
481
660
V_{dd}
Latch
RST
666
486
NCO
663
Pull
down
INV
488
661
487
INV
662
LAT
499
STB
668
664
36
Bit line
Readout
bus
Control &
Timing
498
Memory
Cell
$V_{Th}(i)$
10
Page Controller
GND

FIG. 14

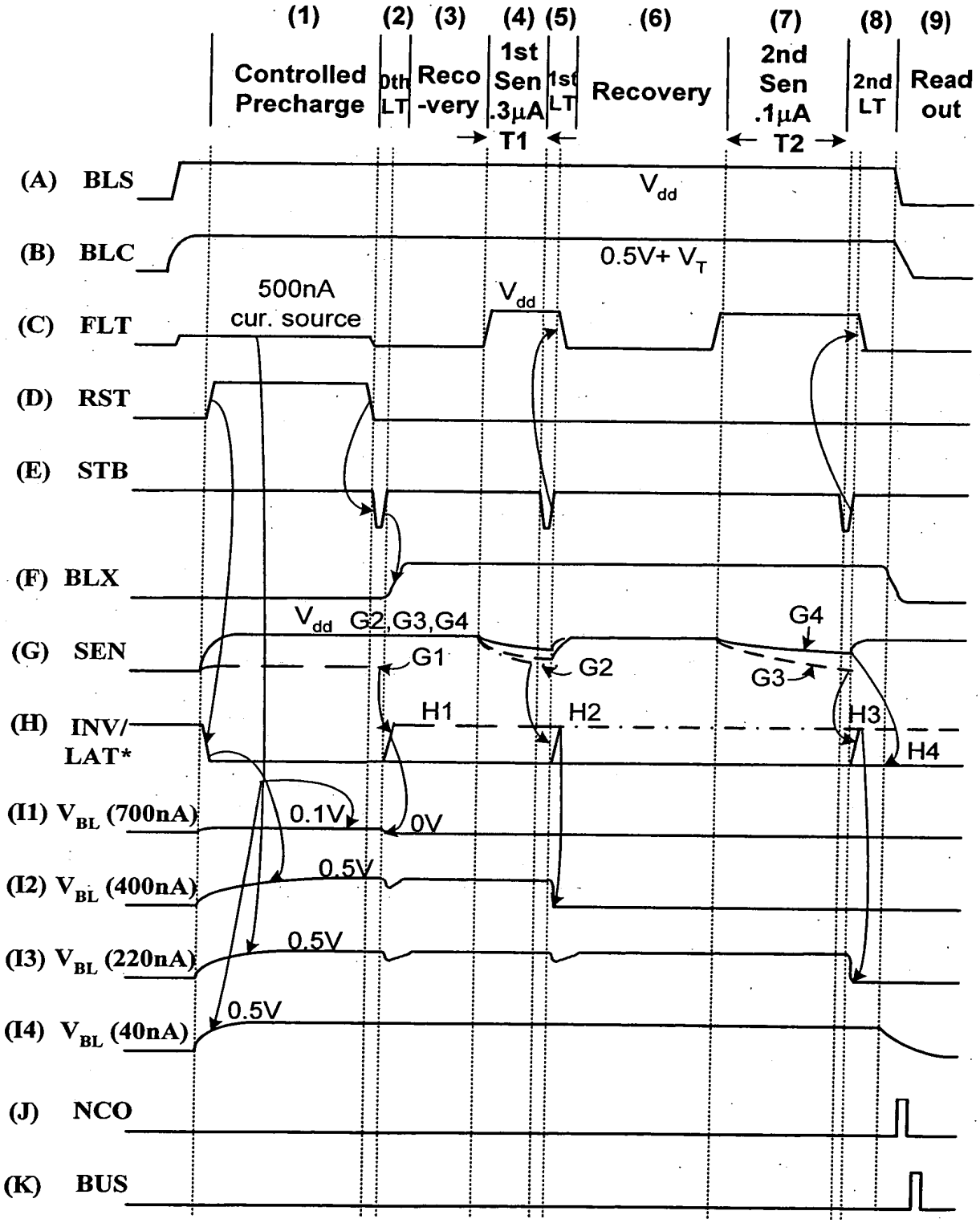

(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
Controlled Precharge
0th LT
Reco -very
1st Sen .3μA
1st LT
Recovery
2nd Sen .1μA
2nd LT
Read out
T1
T2
(A) BLS
V_{dd}
(B) BLC
0.5V+ V_T
500nA cur. source
V_{dd}
(C) FLT
(D) RST
(E) STB
(F) BLX
V_{dd} G2,G3,G4
G4
(G) SEN
G1
G2
G3
H1
H2
H3
H4
(H) INV/ LAT*
(I1) V_{BL} (700nA)
0.1V
0V
(I2) V_{BL} (400nA)
0.5V
(I3) V_{BL} (220nA)
0.5V
(I4) V_{BL} (40nA)
0.5V
(J) NCO
(K) BUS

FIG. 15

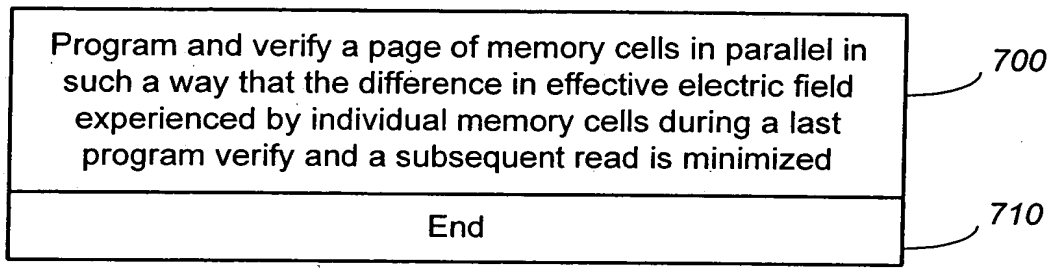

Program and verify a page of memory cells in parallel in such a way that the difference in effective electric field experienced by individual memory cells during a last program verify and a subsequent read is minimized
700
End
710

FIG. 16A

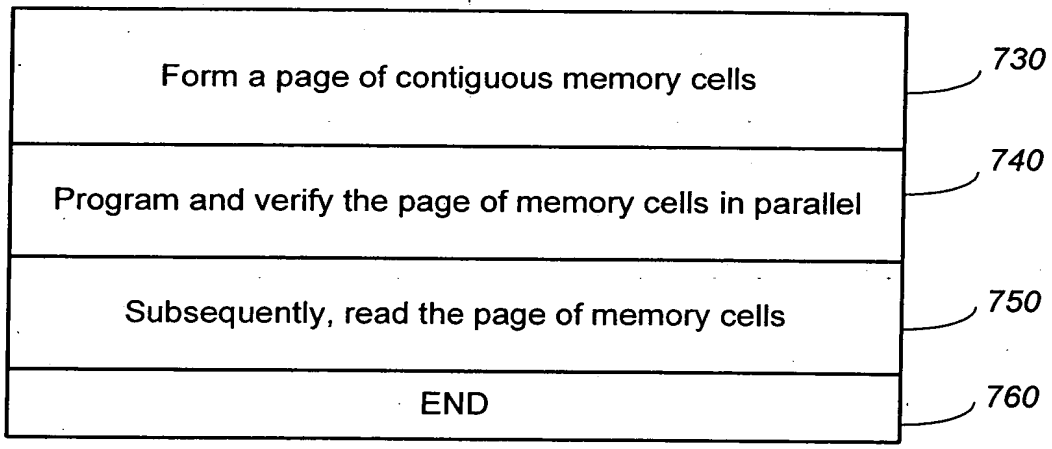


FIG. 16B

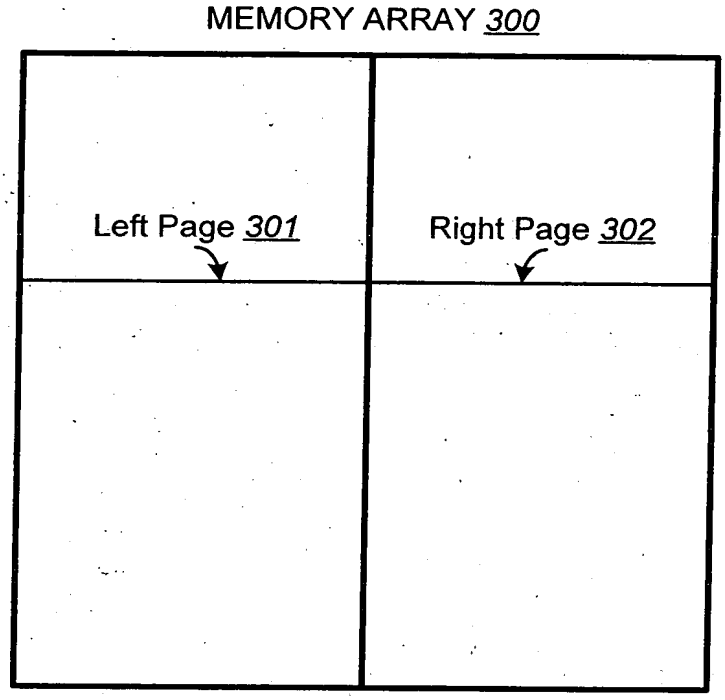


FIG. 17

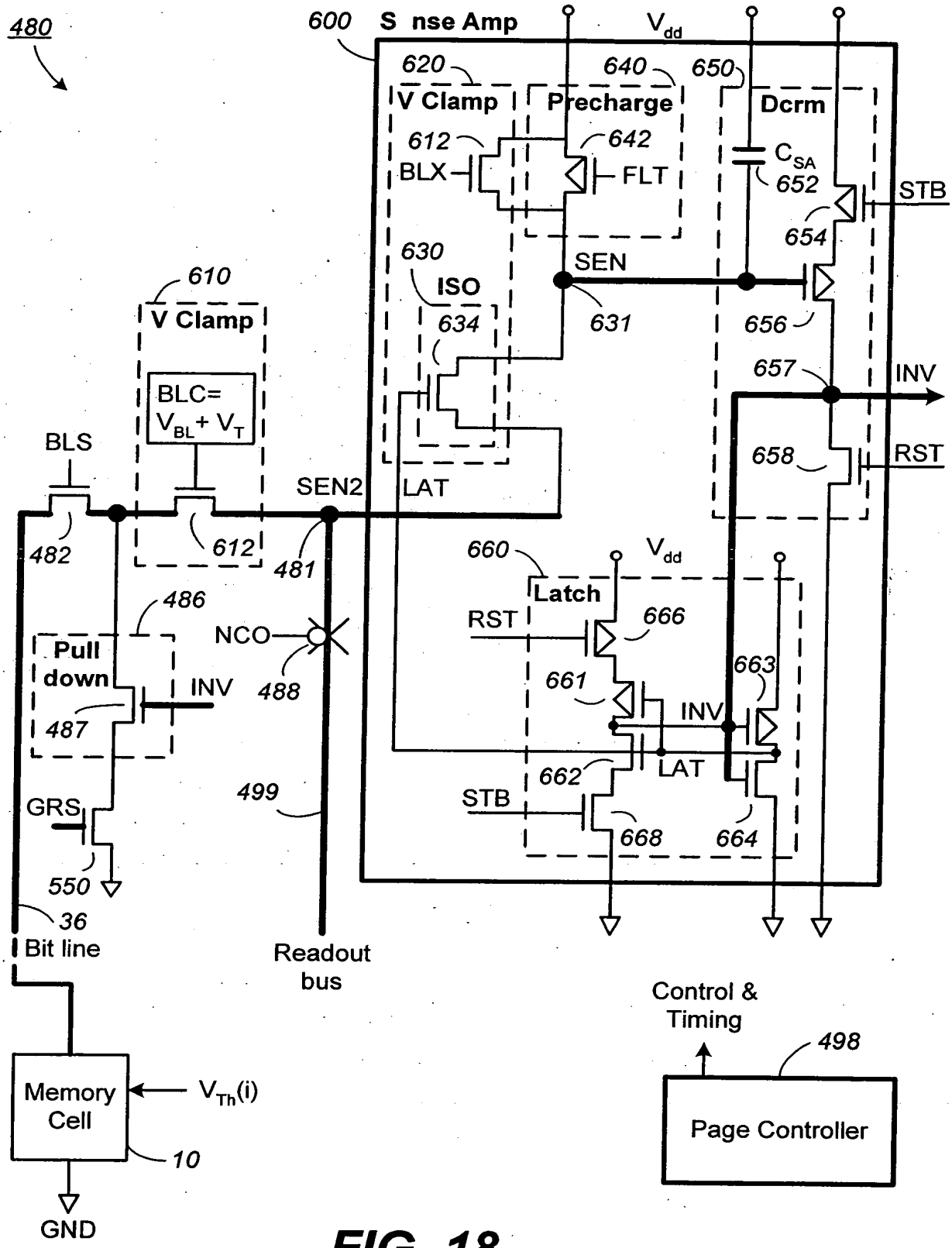

480
600
S nse Amp
V_{dd}
620
V Clamp
640
Precharge
650
Dcrm
612
BLX
642
FLT
C_{SA}
652
STB
654
630
ISO
SEN
634
631
656
610
V Clamp
BLC=
$V_{BL}+V_T$
657
INV
BLS
658
RST
SEN2
LAT
482
612
481
660
V_{dd}
Latch
RST
666
486
NCO
661
663
Pull
down
INV
488
INV
487
662
LAT
499
STB
668
664
GRS
550
36
Bit line
Readout
bus
Control &
Timing
498
Memory
Cell
$V_{Th}(i)$
10
Page Controller
GND

FIG. 18

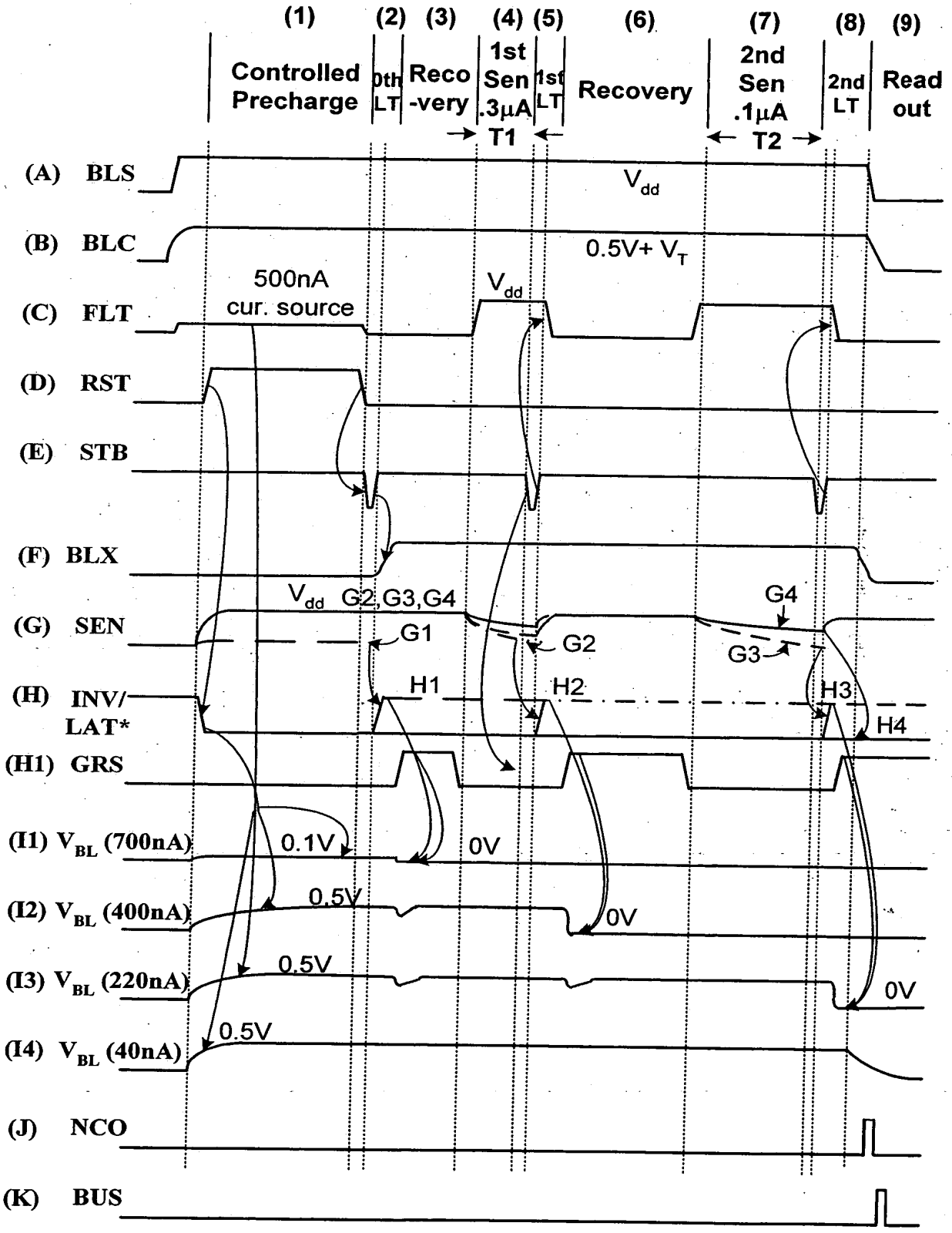

(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
Controlled Precharge
0th LT
Reco -very
1st Sen .3μA
1st LT
Recovery
2nd Sen .1μA
2nd LT
Read out
T1
T2
(A) BLS
V_{dd}
(B) BLC
0.5V+ V_T
500nA cur. source
(C) FLT
V_{dd}
(D) RST
(E) STB
(F) BLX
V_{dd} G2,G3,G4
(G) SEN
G1
G2
G3
G4
(H) INV/ LAT*
H1
H2
H3
H4
(H1) GRS
(I1) V_{BL} (700nA)
0.1V
0V
(I2) V_{BL} (400nA)
0.5V
0V
(I3) V_{BL} (220nA)
0.5V
0V
(I4) V_{BL} (40nA)
0.5V
(J) NCO
(K) BUS

FIG. 19

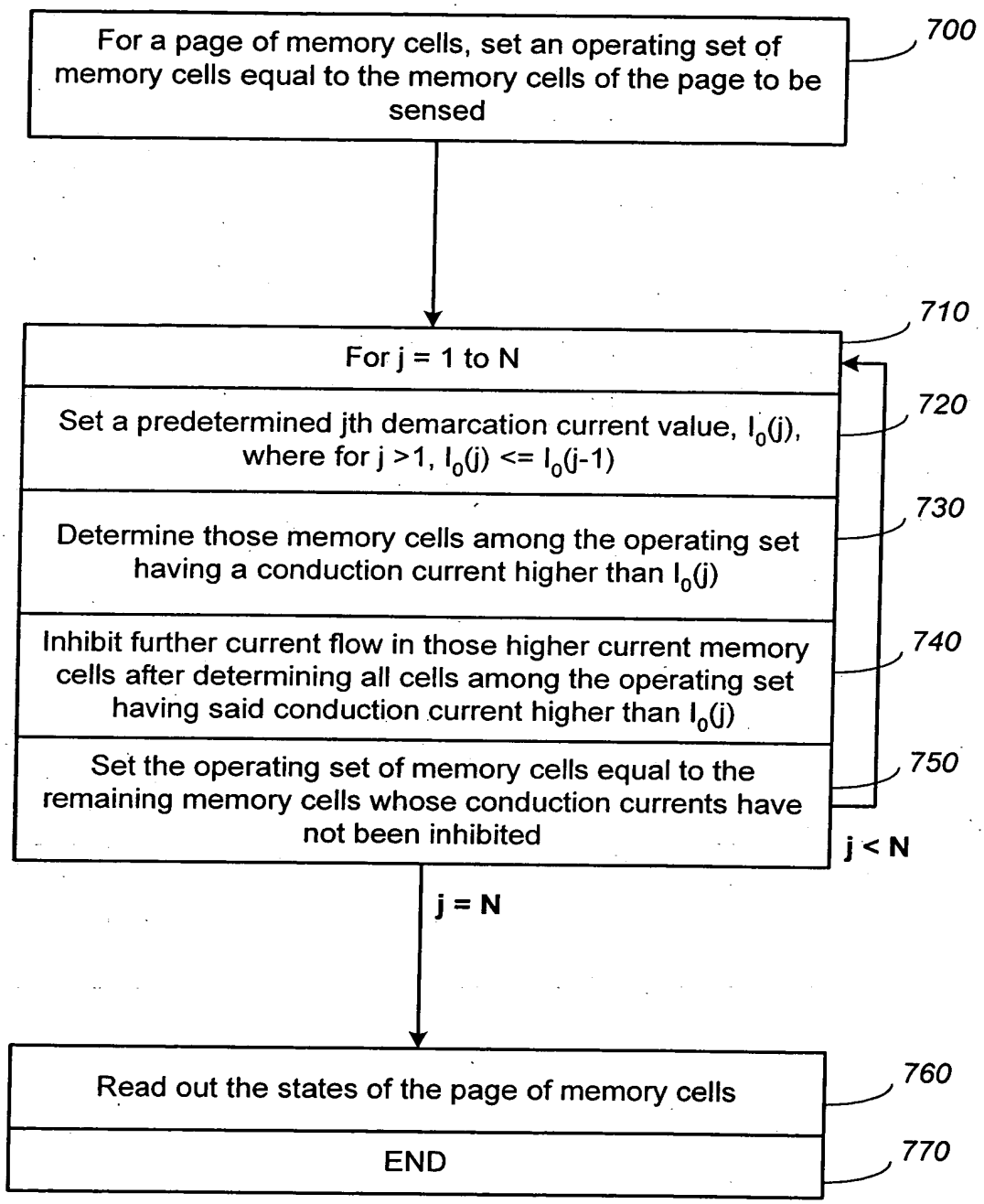

For a page of memory cells, set an operating set of memory cells equal to the memory cells of the page to be sensed
700
For j = 1 to N
710
Set a predetermined jth demarcation current value, $I_0(j)$, where for j >1, $I_0(j) <= I_0(j-1)$
720
Determine those memory cells among the operating set having a conduction current higher than $I_0(j)$
730
Inhibit further current flow in those higher current memory cells after determining all cells among the operating set having said conduction current higher than $I_0(j)$
740
Set the operating set of memory cells equal to the remaining memory cells whose conduction currents have not been inhibited
750
j < N
j = N
Read out the states of the page of memory cells
760
END
770

FIG. 20

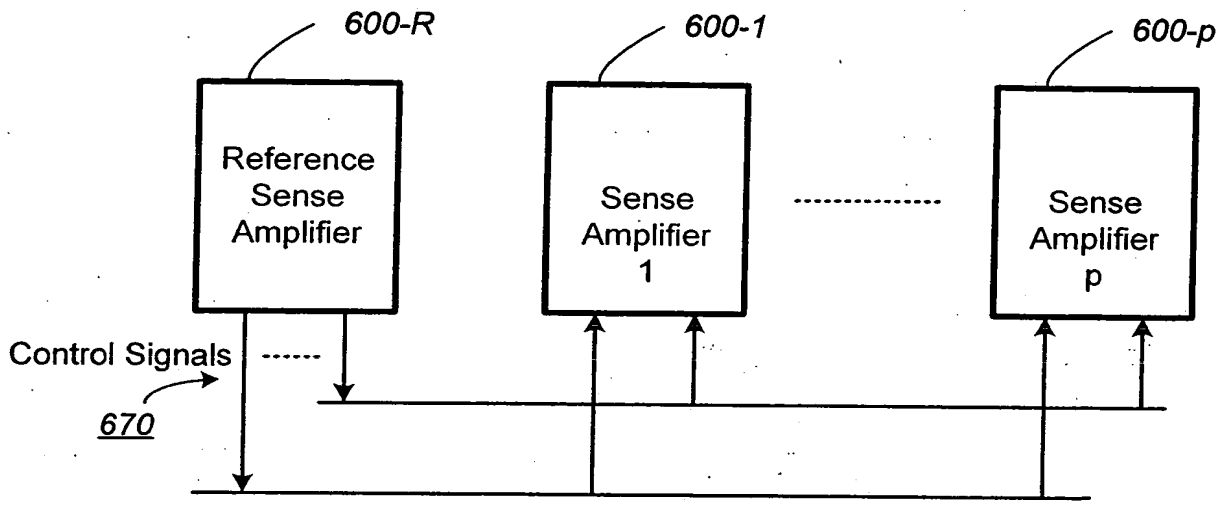


FIG. 21A

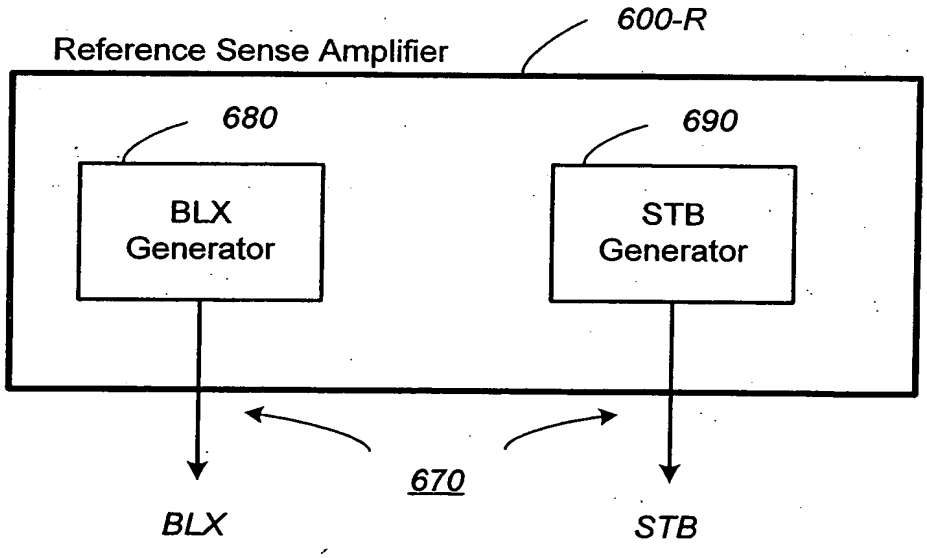


FIG. 21B

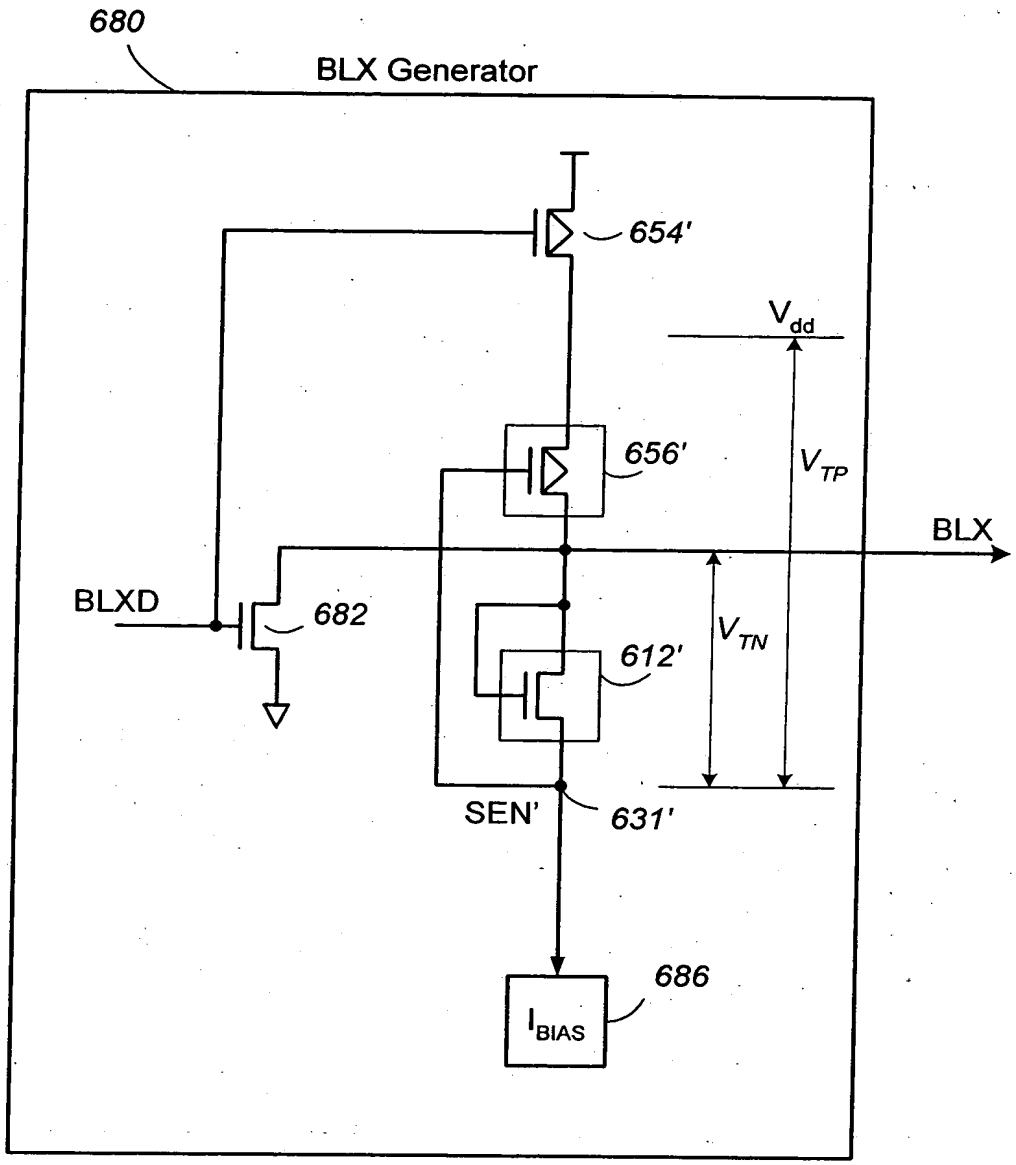

680
BLX Generator
654'
V_{dd}
656'
V_{TP}
BLX
BLXD
682
V_{TN}
612'
SEN'
631'
686
I_{BIAS}

FIG. 22

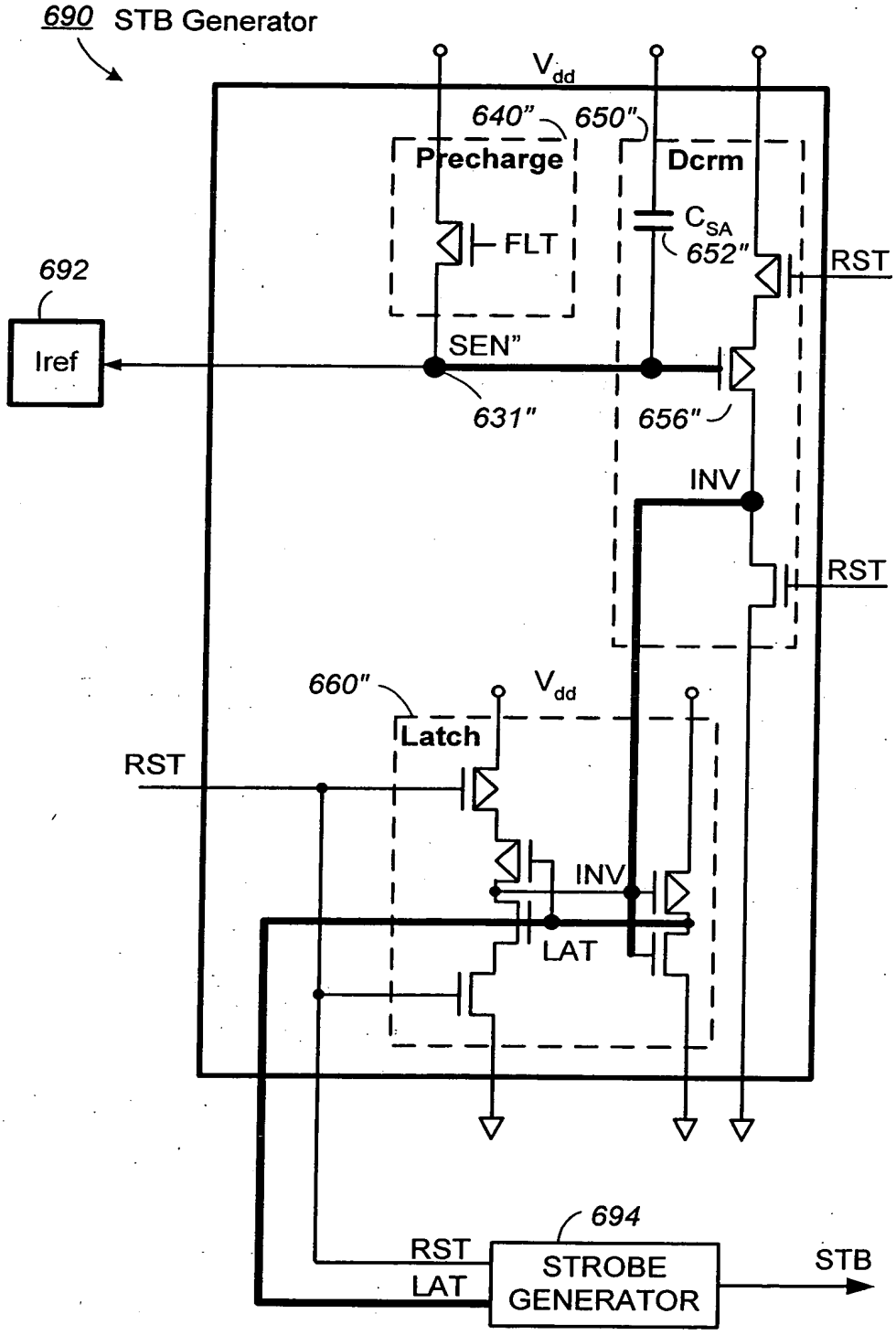

690 STB Generator
V_{dd}
640"
650"
Precharge
Dcrm
FLT
C_{SA}
652"
RST
692
Iref
SEN"
631"
656"
INV
RST
660"
V_{dd}
Latch
RST
INV
LAT
694
RST
LAT
STROBE GENERATOR
STB

FIG. 23